CACHE FOR INSTRUCTION SET ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

A distributed data cache includes a number of cache memory units or register files each having a number of cache lines. Data buses are connected with the cache memory units. Each data bus is connected with a different cache line from each cache memory unit. A number of data address generators are connected with a memory unit and the data buses. The data address generators retrieve data values from the memory unit and communicate the data values to the data buses without latency. The data address generators are adapted to simultaneously communicate each of the data values to a different data bus without latency. The cache memory units are adapted to simultaneously load data values from the data buses, with each data value loaded into a different cache line without latency.